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ARPA NETWORK INFORMATION CENTER
Stanford Research Institute
Menlo Park, California 94025
NIC # 15341
Packet Radio Temporary Note # 40

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19 March 1973

SOME THOUGHTS ON TECHNIQUES FOR BIT SYNCHRONIZATION FOR PACKET RADIO SYSTEMS

1.0 INTRODUCTION

In the design of packet radio systems, we are concerned with at least the three following types of synchronization.

A. Carrier synchronization (coherent systems only)
B. Bit synchronization
C. Packet synchronization (i.e., control of packet transmission times to minimize interference).

In the packet radio group meeting of 2 March, Dr. Fralick suggested that the proper modulation technique to use is QDCPSK. If this other differentially coherent detection scheme, or FM is used, we can dispense immediately with the subject of carrier synchronization under A above. Further, since Note #28 indicated that there exists very little difference in the range performance of any of the systems analyzed, it is suggested that at this stage of the development, the preferred modulation technique be defined as that which results in the most economical hardware. It appears that differentially coherent PSK detection is quite competitive with other techniques such as FM and is far more attractive from an economic point of view than more sophisticated techniques which may offer slightly improved performance. In any event, the choice of modulation technique is not likely to have a significant impact on the techniques to be used for bit synchronization as defined below.

This note primarily addresses the subject of bit synchronization, but to make the presentation more understandable, it has been related to a general terminal model and some important design and implementation problems are briefly discussed in Section 5.

This note suggests that there is no merit considering bit synchronization beyond the period of one packet, though there is some merit in considering synchronization of terminals and repeaters that may contribute interference during the period of one packet. Though this may sound somewhat inconsistent, it is shown below that this

objective can be met with proper frequency control and that the requirements here are quite reasonable at least for the systems with no spread or a system with moderate spread. Such coordination of synchronization between stations is of more value for the system using spread spectrum techniques. In the concept outlined below each packet is considered as a separate transaction and may originate from a different terminal or repeater and have a different time reference. Therefore, if adequate frequency stability is provided, the problem of synchronization is one of accurately defining time and one method of accomplishing this is suggested below, though it has not been analyzed in detail.

Considerable emphasis has been given to the subject of bit synchronization by designers of large networks and solutions generally evolve into the following general categories.

1. Mutual synchronization of the total network by an averaging process.
2. Synchronization to a common master.
3. Use of bit stuffing techniques to remove clock frequency difference between users.

It is important to recognize that these solutions are dictated by the time division multiplexer required : used to separate the various users. The packet radio is not faced with such problems since each packet defines, by means of its address, the proper receive port on the multiplexer. It is, therefore, concluded that there is no merit in considering wide distribution of bit synchronization in the usual sense if there exists little "slip" in the timing over the interval of one packet. This can be achieved with proper attention to oscillator precision and it is shown that the requirements are quite reasonable to achieve at least for systems with no spread or with moderate spread factors. It is also shown that the stability requirements are a function of packet length and are not a function of data rate. The hardware implementation of the concept is also briefly outlined. If there is sufficient traffic density through a repeater of either real or artificial nature, it may be desirable to maintain terminals in the region of a particular repeater in continuous synchronization with the repeater to simplify the oscillator design requirements for the low cost terminal. The subject of

bit sync requirements and its relation to interference reduction and processing gain in spread spectrum systems has been addressed in more detail in packet radio note #33.

2.0 GENERAL CONCEPT OF BIT SYNCHRONIZATION

Consider a network of repeaters and terminals with maximum spacing of 10 miles. If the system is operated at a data rate of 100 kb/s with bi-phase modulation the symbol period is 10 microseconds and the clock rate is 100 KHz. Transmission time for the 10 mile path is approximately 54 microseconds, hence the beginning of the message is received about 5.4 bit periods or almost 2000 degrees of clock phase after the start of transmission. For detection purposes however, we need only be concerned with clock phase over a range of 360°. If we wished to synchronize such a network, a time or phase reference could be established for each terminal and repeater which is referred back to some control point such as a station. Each terminal and repeater would then be required to predict the required phase at time of arrival at the repeater to which a message is addressed and adjust the transmit phase accordingly. Such a technique is used for time slotting of messages in TDMA satellite relay systems where the central time reference is at the satellite. However, the complexity of controlling sync among a number of stations in the packet radio system quickly convinces one that this would not be a satisfactory technique for maintaining bit sync, though a similar technique still may be considered as a method of message slotting.

The alternate and obvious approach is to synchronize independently to each packet. This is likely what everyone had in mind in the first place but the fixed time reference concept was summarized above to emphasize that continuous network synchronization is complex and probably of little value for packet radio systems. For packet radio the problem can be reduced to one of epoch determination for each packet. If we can design all clocks to run at sufficiently constant rate independent of external control, then epoch determination from a transmitted preamble is adequate for synchronization. In other words, all we need to do is set our clock at the beginning of each packet. For this system, our "day" is 10 microseconds long; and no transaction extends beyond 1000 "days" on our calendar. We are only concerned with the

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time of day a particular transaction started, and for convenience we reset our clocks to midnight at the beginning of the transaction and let it run at a predetermined rate from that point.

2.1 Summary of Characteristics of Suggested System

a. All stations are bit synchronous in the concept that during the period of one packet the "slip rate" is a small fraction of a bit once the time reference (epoch) is established. (i.e., all clocks have accurate rate but are arbitrary in phase.)

b. Epoch is established by a preamble and once established, timing is not corrected during the packet transmission.

c. Epoch is re-established for each packet transmission.

d. Transmit clocks at both terminals and repeaters are phase independent of receive clocks through derived from the same time base. (This allows synchronization of terminals to a particular repeater should this prove desirable.)

The approach outlined above resolves down to one of accurately resolving a time reference (phase) during a defined preamble and accurately maintaining frequency once phase is set. No phase correction is made once phase is established. The argument for this approach is summarized below:

a. Timing must be accurately established by the beginning of the header if header is to be accurately decoded. There is little merit in further correction (by use of phase lock loops) if slip rate requirements are reasonable.

b. Preamble may be designed for optimum bit sync acquisition. While it is desirable that no restrictions be placed on the message or header content (i.e., may contain all zeros if we so desire). In a practical system phase of bit recovery is influenced by bit pattern.

c. The system allows use of the same master clock for outgoing or incoming information.

d. Master clock may be of high precision since it is not required that it be adjusted in frequency as part of an analog or digital phase lock loop. Phase adjustment is made using techniques that do not influence clock long term frequency stability.

2.2 Oscillator Stability Requirements, System With No Spread

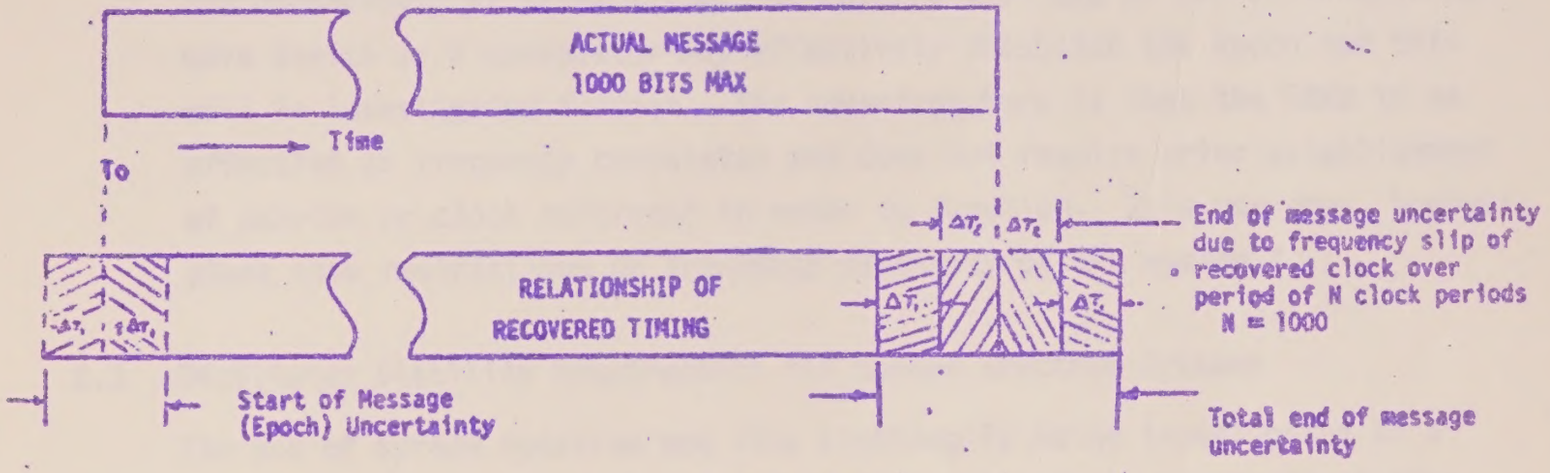


FIGURE 1

Assume following tolerances on timing:

Accuracy of estimating of Epoch = 12° of clock phase (.33 μ sec for 10 kb/s system)

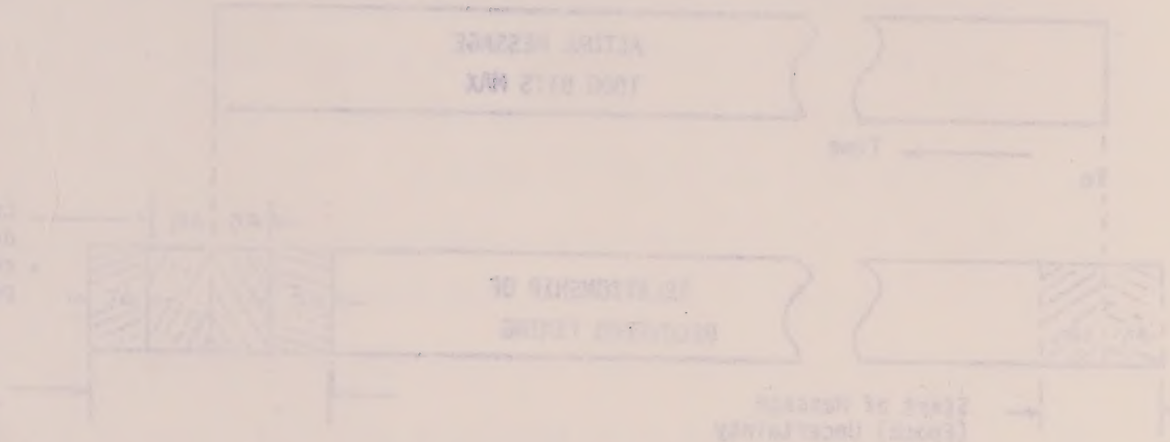
Maximum slip in clock phase over 1000 bit packet = 6° of clock phase

The above values seem reasonable although they have not been evaluated in terms of loss in error threshold.

If the maximum packet length, including header, is 1000 bits then oscillator accuracy to meet 6° slip is:

$$\text{Clock Accuracy} = \pm \frac{1}{1000} \times \frac{6}{360} = \pm 1.66 \times 10^{-5}$$

Since both transmit and receive clocks are involved in this tolerance, the accuracy of each clock must be twice the above value or about 8 parts per million. If n = 100 then the clock can be set to nearest $\frac{1}{100}$ of clock cycle or 3.6° (this can be improved by a factor of 2 by using both positive and negative transitions of the clock cycle). This, then, leaves about 8° error in determining the Epoch. The ability to meet this requirement is related to preamble length, signal to noise, and signal dispersion due to reflections. However, it appears that if S/N is adequate to achieve a



bit error rate of 10^{-5} (packet error rate of 10^{-2}) it should be possible to achieve desired sync accuracy with a relatively short preamble.* False alarm rate under no signal conditions may be a more important consideration. The system must operate with a wide dynamic range of signals, hence epoch detector must be able to operate in a Gaussian noise environment with a low probability of false alarm. It appears that use of surface acoustical wave device as a correlator may effectively establish the epoch and this will be investigated further. The advantage here is that the SAWD is an effective IF frequency correlator and does not require prior establishment of carrier or clock reference in order to function. It's use does, however, place some restrictions on frequency stability of the system.*

2.3 Oscillator Stability Requirements for Spread Spectrum Systems

The use of spread spectrum and time slotting is being investigated as a means of sorting multipath and interference signals on the basis of time of arrival. This subject is covered in more detail in Note #33. With spread spectrum systems, accurate establishment of epoch and good bit sync stability is an important consideration, particularly if this technique is used to separate signals on the basis of time of arrival.

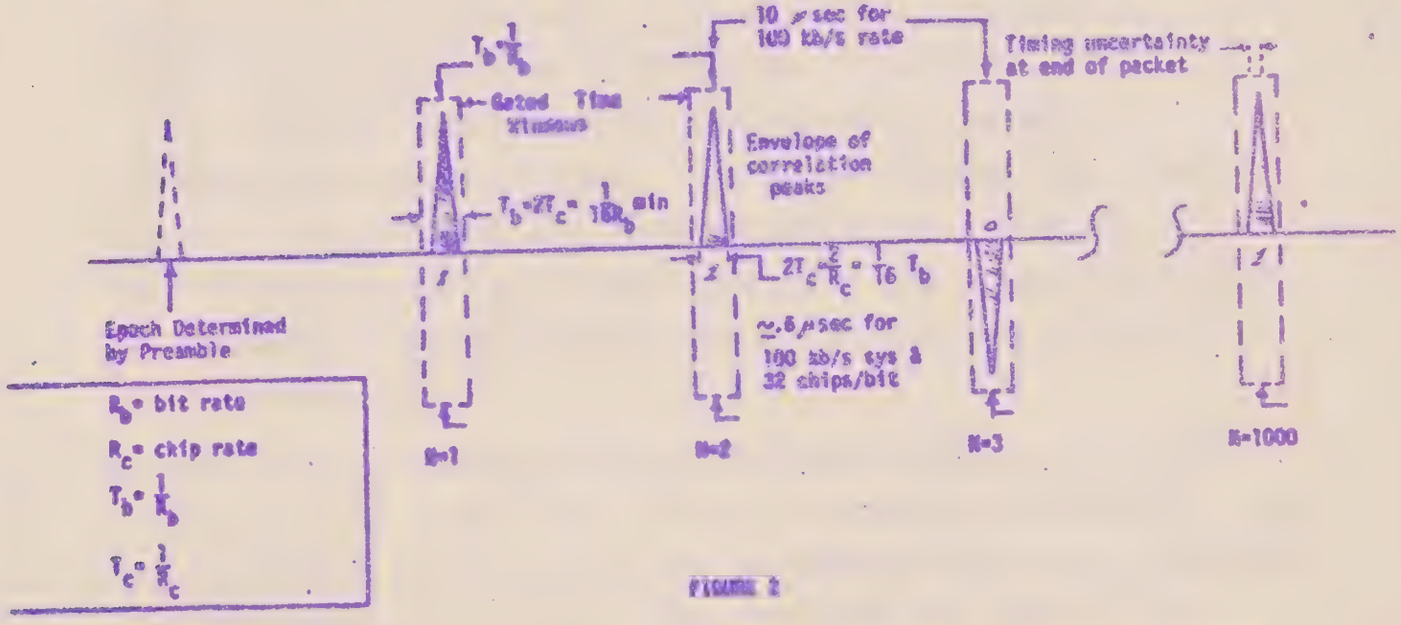


FIGURE 1

Consider the model outlined above. The data symbol for zero is a PRN sequence, PRN_1 and symbol for one is an orthogonal sequence PRN_2. It is

*See note #33 for more detail on preamble and frequency stability requirements.

convenient, though not necessary, to make $PRN_2=\overline{PRN_1}$, and use differential detection. This allows use of only one code for the surface wave lines to be used in the receiver (see Figure 2-2 in Note #33). If the sequence is 32 bits long, the bit rate = R_b and biphase modulation is used, then period of sequence 1 = $1/R_b$. (The chip rate is 32 R_b and chip period is $\frac{T_b}{32}$).

The correlation peak for PRN sequence is 2 chips wide at the base; therefore, if we can accurately define epoch, then we cam sample the signal through a time gate of width no longer than $\frac{T_b}{16}$. By this technique all interference occuring outside this frame may be disregarded. Therefore, if other stations transmit at random, the probability of a given interferor falling on the desired slot is $1/16 \simeq .06$. However, this probability exists only if interfering signal is exactly in sync. If two clocks slip by one cycle over packet length of 1000 bits (i.e., one transmits 1000 bits in a period and the other transmits 999 or 1001), then there is a probability of 1.0 that at least 1 bit interference will occur if both start transmitting at about the same time. However, 10^{-3} clock stability is very poor and we can certainly do better.

> Note: The signal need not necessarily be time gated if the detection is accomplished by sampling the value at precise time intervals since time selection is accomplished by the sampling process. However, signal may also be selected by a time gate of some defined width and the value of the signal within the gate integrated over the period of the gate by integrate and dump techniques. The second approach may allow poorer clock stability and epoch determination. Also, multi-path characteristics are almost sure to effect the optimum choice of detection technique and the need for further evaluation is clearly indicated.

For this model it would seem reasonable to allow a gate position drift of 1/4 of a chip interval. This then results in a total gate width of 2 1/2 chips plus any further allowance that may be required for error in defining epoch. For this model the framing of the first and last pulse of the packet is shown for zero epoch error in Figure 3 below.

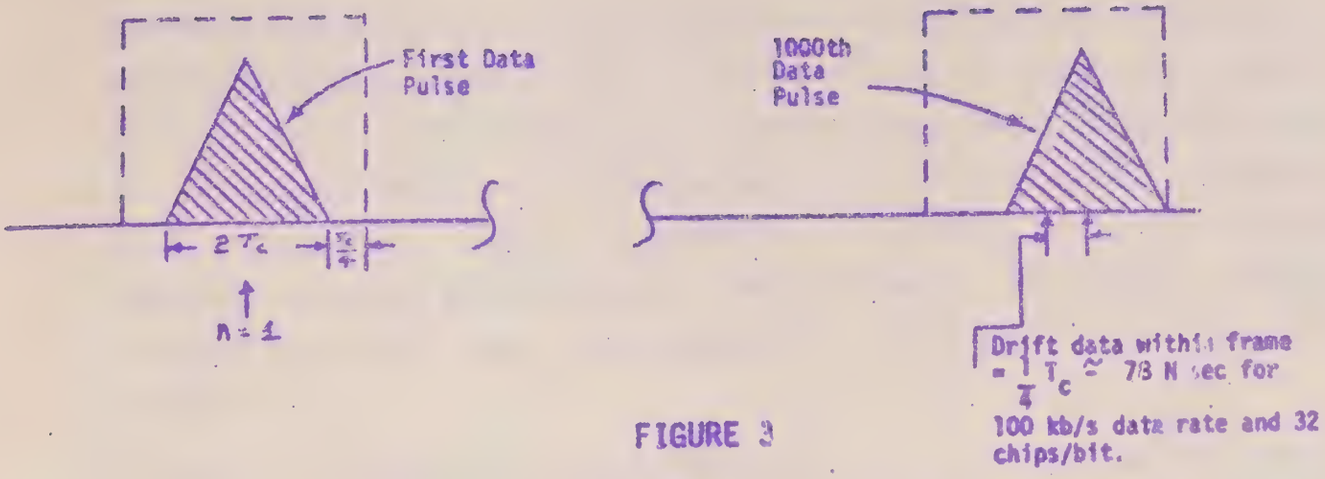


FIGURE 3

For this example the clock time is allowed to drift 1/4 chip period or $1/32 \times 1/4 = 1/128\, T_b$. (Where T_b is bit period). Since two clock oscillators are involved, the accuracy should not be worse than $1/2 \times 1/128 \times 1/1000 \simeq 4 \times 10^{-6}$. This is only twice the stability calculated for the non-spread system. No allowance has been made for epoch error but for spread system this is expected to be small <u>if</u> multipath is not severe. (See Note #33.) Also some of the skirts of the correlation peak may be clipped without significantly affecting the total energy under the correlation envelope. In fact, in transmitting through a reflective or dispersive medium, there may be some advantage in narrowing the window through which the correlation peak is sampled.

It will be noted from above that required stability is a function of packet length and a function of chips per bit, but is not a function of bit rate.

3.0 OSCILLATOR REQUIREMENTS

The stability and aging characteristics of crystal oscillators vary at least two orders of magnitude with differences in the cut of crystals and choice of oscillator circuit[1]. However, stabilities in order of a few PPM can be obtained with a well-designed temperature-compensated oscillator and better stability is possible if precision ovens are employed (See Appendix).

Therefore, it appears that adequate stability can be obtained with carefully temperature compensated crystal oscillators if only moderate spread factors are used. Further, the tolerance that may be allowed

for the clock frequency of the hand held terminal may be essentially doubled by placing much tighter requirements on the repeater. Such an approach is not unreasonable since temperature stabilized crystals may be used at the repeater without paying a significant price in terms of power consumption. Such an approach is not attractive for the terminal since the terminal may be operated intermittently and crystal oven warm-up times make their use unattractive for a unit that is operated intermittently.

If precision temperature controlled oscillators are used at each repeater, it may be more economic to synchronize each terminal clock to a repeater if sufficient traffic through the repeater is assured to allow reliable synchronization. The terminal need not transmit to the same terminal from which it receives sync, though there appears to be some merit to synchronizing the terminal to the strongest repeater and then transmitting its traffic to that repeater. If the terminal cannot lock to a repeater, then there is no merit to transmitting, hence, such an approach leads to confidence that the system is working prior to an attempt to transmit. Such an approach would require rather slow clock loops since it must hold with little slip over at least its transmit period of 1000 bits. This implies clock loop band width well below 100 HZ for the 100 kb/s system or some form of sample and hold technique. Since the frequency errors to be corrected result from temperature and aging, it appears that once the required correction was determined, it could be held for long periods. Such a time gated AFC system with long hold periods merit further investigation if adequate stability cannot be acheived by simpler techniques.

4.0 DOPPLER

For the simplified timing model described above, the timing accuracy required over a packet period was about 40 n sec for the system with x32 spread and about 80 n sec for the non-spread system.

> Note: These values were for a reasonable though somewhat arbitrary system models, hence little significance should be given to the ratios of the above two numbers for the two quite different models.

Doppler is a time expansion or compression phenomenon, hence the maximum relative velocity allowed is that which results in a 40 n sec time expansion or compression during a packet in time of .01 seconds (1000 bit packet at 100 kb/s assumed), hence:

$$V_{max} = c\,\frac{\Delta t_2}{T_p} = \frac{1.86\times10^{5}\times40\times10^{-9}}{10^{-2}} \simeq 0.74 \text{ miles/sec} \simeq 2680 \text{ miles/hr}$$

Where: c=velocity of light

t_2=allowed timing error at end of packet

T_p =time duration of packet (.01 sec assumed i.e. 1000 bit packet at 100 kb/s).

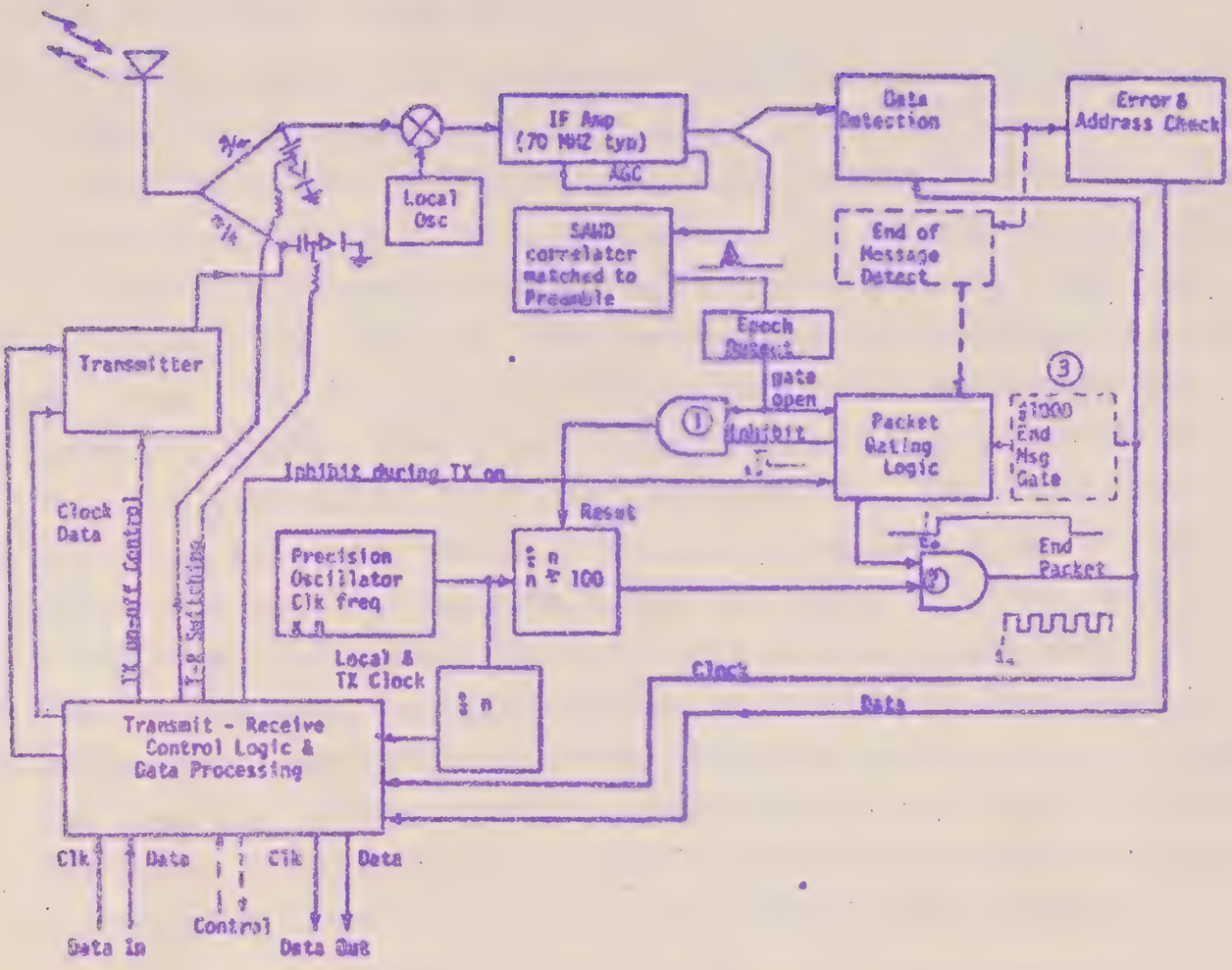
It is therefore concluded that doppler will not present a significant timing problem for packet radio systems even if operated from jet aircraft.

Note: For systems using spread techniques, the doppler frequency error may be a more important consideration. See Note #33 for relationship between bit time (T_b) and allowed frequency error if surface wave devices are used to decode the data symbols.

5.0 TIMING RECOVERY IMPLEMENTATION

5.1 Circuit Description: A simplified block diagram of a packet transeiver is shown in Figure 4. This diagram gives emphasis to one possible implementation of bit timing.

A surface wave correlator matched to the preamble is used to determine epoch. In the arrangement shown, this is accomplished independent of the circuits that decode the data. The technique is applicable to both spread and conventional non-spread PSK systems. The preamble correlator output pulse defines epoch , initiates the packet gating circuit and resets the counter following the precision oscillator. The packet gate is open for the full period of the message. This gate inhibits any further reset of the counter regardless of the output of the preamble correlator and feeds bit sync to the data detection and output circuits. If the packet does not contain end of message information, this must be obtained by some technique from the signal detection circuits or for a



Notes

1. Gate passes only epoch pulse that occurs prior to opening of packet gate. Packet length gate is delayed sufficiently to ensure that counter has settled following reset. No further reset is then possible for duration of packet length inhibit.

2. This gate passes clock pulses only after a packet gate is open.

3. If packet lengths are fixed (i.e., 1000 bits) then end of message may be defined by countdown as shown

Figure 4

Simplified block diagram of transceiver and modem showing timing recovery using surface wave correlator to recognize preamble.

FIGURE 4

system with fixed packet lengths the packet gate closing can be initiated simply by counting the proper number of clock pulses.

5.2 Misc. Circuit Design Requirements

5.2.1 IF Amp and AGC: It is necessary that the receiver be capable of handling a wide dynamic range of signals. It is also necessary for the receiver to recover rapidly following transmission of packet if maximum transmission efficiency is to be obtained. The receiver recovery characteristics will determine the allowed leakage of transmit signal into the receiver and hence will influence the cost of the transmit-receive switching. Since the system should be designed to operate near the noise threshhold, it may be necessary to include some protection in the correlator against false epoch determination. This is of most importance for spread systems since total signal energy may be below total noise energy at the input of the correlator. For the unspread system, the IF AGC and/or limiter maintains the IF output constant down to full noise level. Since there is no point in detecting epoch unless S/N is about 10 db or better (because of error rate requirements) and since the .001% noise peaks of gaussian noise are about 13 db above RMS noise, it should not be necessary to have much processing gain to achieve a low false alarm rate for the unspread (DPSK) systems.

5.2.2 Epoch Determination: Though use of surface wave correlator appears to offer a means of rapidly synchronizing to the preamble of the arriving packet, there are implementation problems associated with this approach. An 8 bit preamble would require an 80 microsecond delay line for a bit rate of 100 kb/s. This is beyond the delay that can be economically fabricated, hence may require use of two or more devices to achieve economic implementation. For this reason, more conventional bit acquisition techniques (i.e. phase lock loops) are to be investigated in order to establish a baseline against which performance and cost of other techniques can be evaluated.

5.2.3 Transmitter and Antenna Switching: A simple technique of transmitter-receiver switching is shown in Figure 4. The degree of isolation required between the transmitter and receiver will be influenced by receiver design, Particularly the response of the AGC system. It likely will be necessary

to use more than one diode in the receive line to achieve increased isolation. Shunt diodes would be spaced at 1/4 λ intervals. Series Pin diodes may also be used to increase isolation. In order to minimize effect of T-R switches on receiver noise figure, it may even be desirable to include some switched attenuation in the IF amplifier. It also appears advisable to provide some receiver overload protection at receiver input to prevent receiver damage in event failure occurs in transmit receive logic. It will be noted that switch is not RF operated as is common in radar systems, but receives switch commands from T-R logic unit. The complete T-R switching system may be implemented with stripline techniques. The mixer may also share the same substrate.

The T-R control also must switch power to the transmitter. Power to all stages requiring significant power should be switched in order to achieve maximum efficiency. Decoupling requirements may introduce some lag both in turn-on and turn off cycles. Rapid turn on might be implemented using an SCR to transfer charge from a large capacitor to the smaller bypass capacitors. Rapid turn off might be implemented by "crowbar" techniques which employ SCRs to rapidly dump the charge on the bypass capacitors in the transmitter. Since duty cycle is quite small it appears that relatively small and economic SCR's may be used even for systems that may have power outputs in order of 20 watts.

5.2.3 End of Message Determination: If messages of variable length are to be handled, it is necessary that some technique be employed to define end of message and remove the inhibit from the epoch detector to ready it for the next packet. If the system is to operate with only one set of characters, (i.e., ASCII) then an end of message may be included in the signal transmitted. Another possible technique is to include the message length in the address. If length is limited to only 4 possibilities, then message length can be defined by 2 bits. These would then set the end of message counter. Signal sensing techniques might also be used but this is not viewed as a very reliable technique at low S/N.

5.2.4 Error and Address Check: Some form of message error check must be made at the receiver. Also the address must be read to determine if the message is addressed to the terminal, repeater or station receiving the message. If the header is not correctly received or is not addressed to the

terminal receiving the message, there may be some merit in closing the packet gate at the point such determination is made and remove the inhibit on the epoch detector. Such an approach has most merit in spread systems since it may allow reception of overlapped packets. However, even in non-spread systems, this would allow rapid reset upon false sync detect and therefore could influence the length of preamble required for satisfactory bit synchronization.

5.2.5 Transmit, Receive Control Logic and Data Processing: The block shown in Fugure 4 was intentionally left vague since requirements are not well defined. However, it is clear that more functions will be required at a repeater than at a terminal. For example, at the repeater, the complete packet must be stored prior to re-transmission and it may be desirable to even provide storage for more than one packet.

It is believed that in defining a functional model, we need to define at this stage primarily the input output functions and basic operational requirements while leaving the logic functions variable since considerable flexibility here may be desirable depending on the class of terminal, repeater or station.

5.2.6 Precision Oscillator & Clock Counter: Though the precision oscillator does not present a severe design problem, the devices and techniques should be chosen with some care. Temperature-compensated rather than temperature-controlled oscillators are recommended for at least the terminal. Stability requirements are influenced to some degree by the degree of spread that may be used.

The diagram shows a countdown by at least 100. Amount of countdown places a fundamental limit on the accuracy of timing if the proposed synchronization technique is used. However, there is no merit in making the timing uncertainty due to frequency division much smaller than that due to epoch uncertainty. This subject requires further investigation. There is no problem in providing higher orders of countdown if required. However, since oscillator frequencies in the range of 5 to 10 MHZ are most favorable to high stability, it might prove desirable to multiply the oscillator signal prior to countdown if division ratios greater than 100 prove necessary.

6.0 CONCLUSIONS

For packet systems, bit synchronization may be reduced to the problem of epoch determination if packet length does not exceed 1000. Such an approach results in reasonable oscillator stability requirements. Stability requirements increase with packet length but are independent of data rate. Further data on achievable stabilities for crystal oscillator is included in the appendix.

The clock oscillator stability requirements are also influenced by the degree of spread used, if any, and will be influenced by the manner in which the data is sampled and the error rate threshhold degradation to be allowed for timing errors. These subjects have not been analyzed in detail in this note since the primary purpose in the preparation of this note was to present a basic concept. Further analysis is intended in order to define detailed specification for the system.

References:

Gerber, E. A. "State of the Art - Quartz Crystal Units and Oscillators" Proc. IEEE, Feb., 1966 pp 103-115.

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9 April 1973

APPENDIX TO NOTE #40
CRYSTAL OSCILLATOR STABILITY

When defining the requirements for a crystal oscillator, the factors that must be specified are the short term, long term and temperature stability rates. The short term stability is generally a function of the drive level with greater drive giving better short term stability but poorer long term stability. The long term stability is basically a function of the cleanliness of the manufacturing process with the limiting factor being that greater cleanliness is more costly. High stability crystals must be manufactured in clean rooms with purity to the molecular level. In ordering a crystal oscillator, the exact parameters must be specified; for example, 1 pp 10^{10} in a period of 10 ms, 1 pp 10^{8} per day and 5 pp 10^{7} over a specific temperature range. For long term stability, the per day measure is generally the standard for the industry. The frequency for maximum stability is 5 MHZ. Designing to this frequency results in a crystal of optimum physical dimensions for achieving the best stability.

The specification for long term stability such as 1 pp 10^{8} per day defines the steady state value following an initial stabilization period. This is as shown in Figure 1.

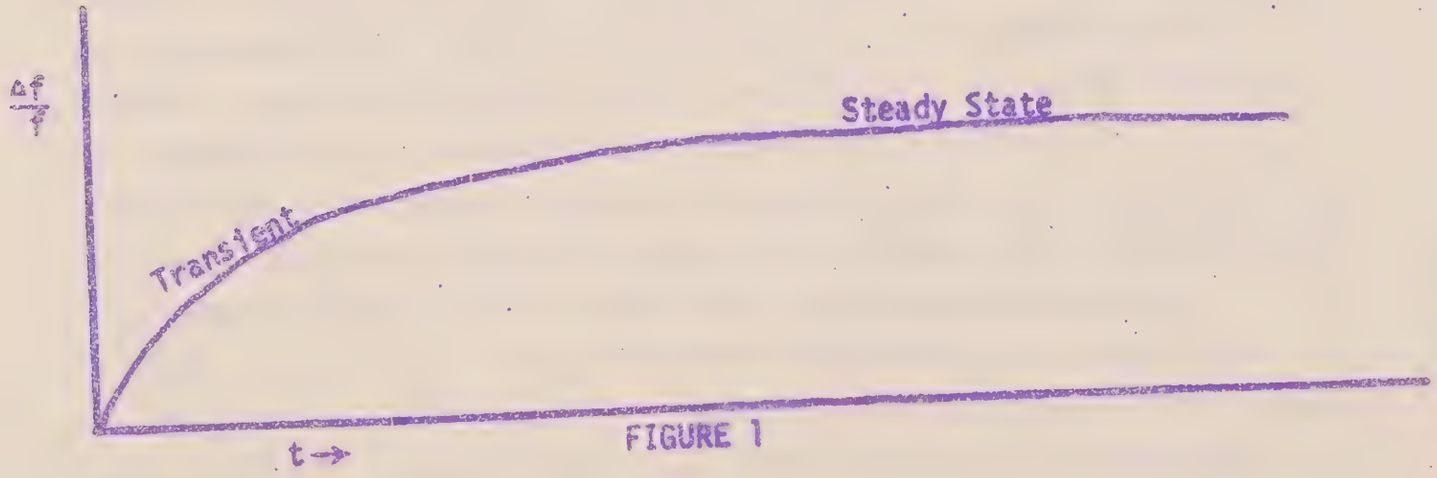
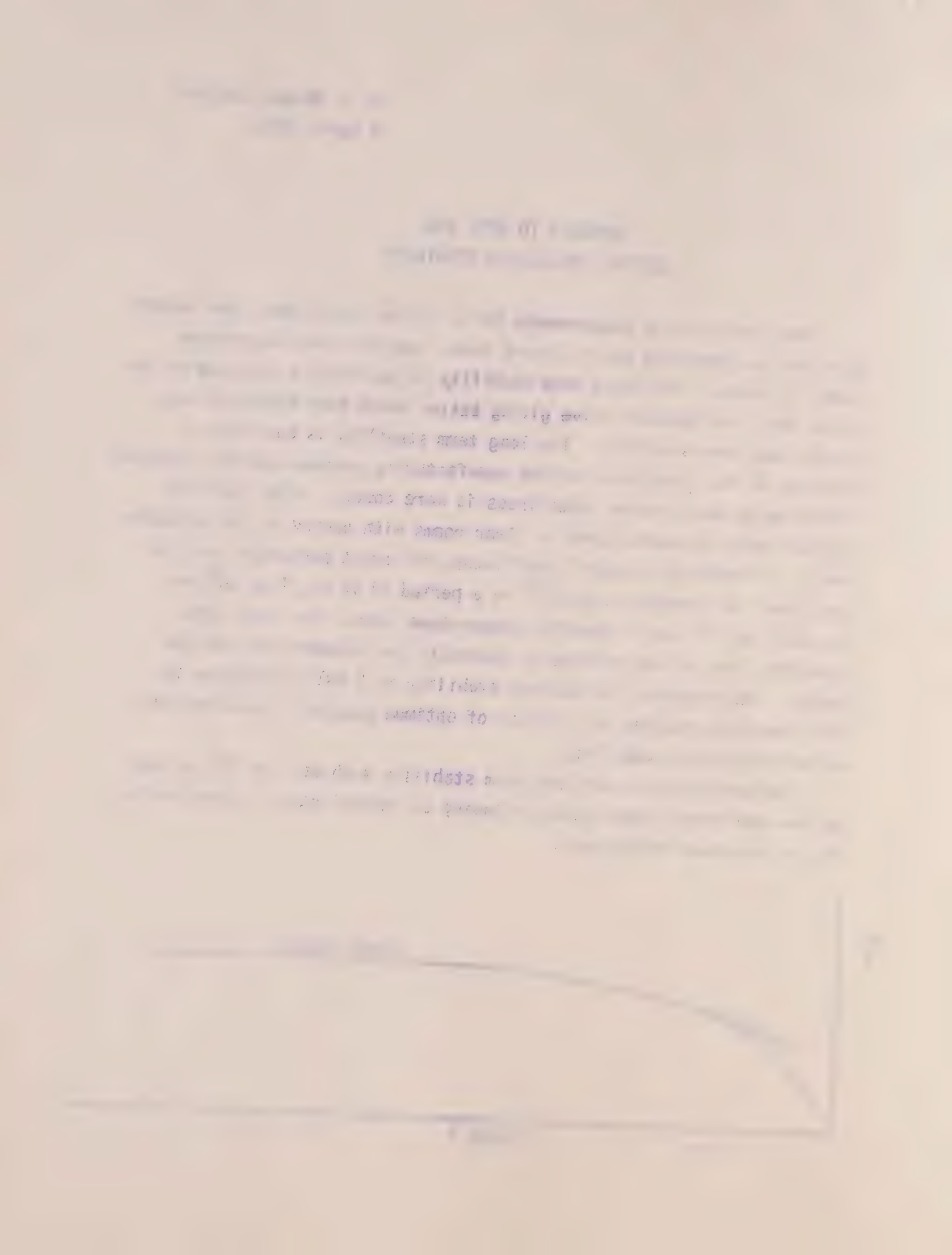


FIGURE 1



The length of the transient period is basically a function of the cleanliness of the crystal; therefore, the crystals with the more stringent long term stability rates have shorter transient times. These transient times can vary from a few hours to a month. Drift rates are generally not defined for the transient period. The crystal likely will follow the transient curve each time it is turned on and it does not necessarily restart at the initial frequency. Two possibilities of operation are shown below.

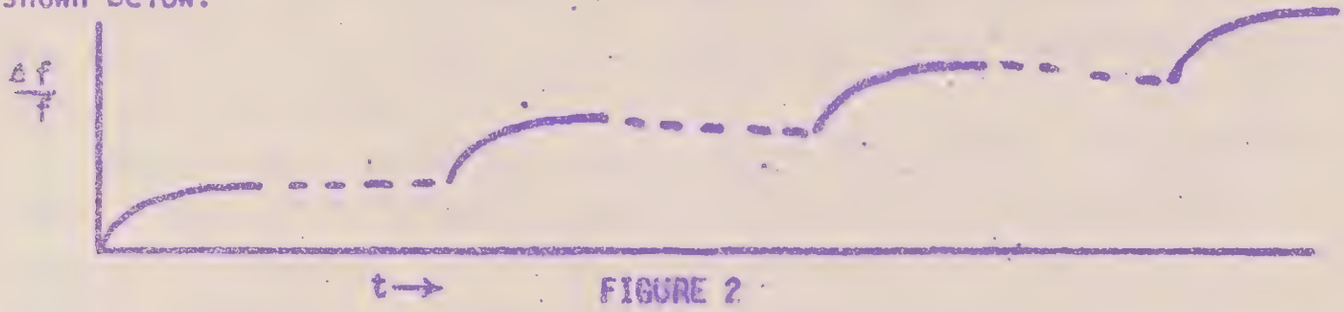


FIGURE 2

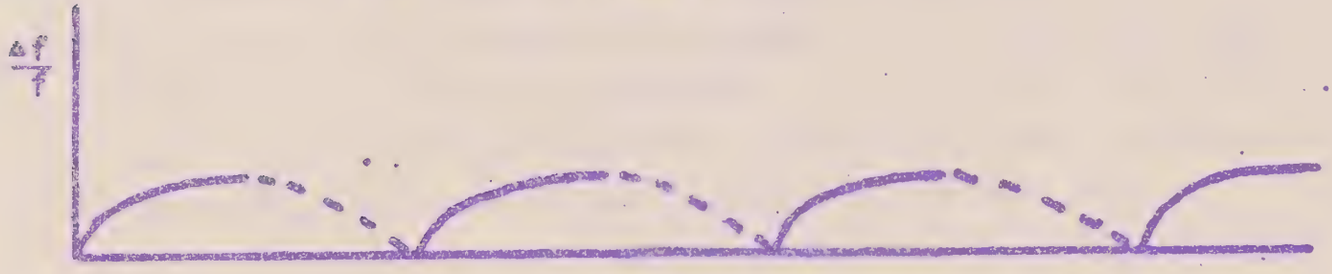


FIGURE 3

If a crystal oscillator has only a minimum margin in long term stability, a drift problem could arise over a long period. Most crystals age in the positive direction.

For the packet radio system, the stability requirement could be primarily a short term matter. A 1 pp 10^8 per day drift rate can be readily achieved and, with this, the hand held unit could maintain a frequency rate very close to that of the repeater. The daily drift rate can be specified to the point that the long term stability factor can be made small as compared to the drift due to temperature change. A reasonable value for frequency stability as a function of temperature change over a range of -40 to +75°C with temperature-compensation circuitry is 5 pp 10^7. A short term stability over a period of 10 ms of a few parts in 10^{10} is possible with current technology. All of these figures pertain to crystals operating near 5 MHZ which are reasonably-

priced production devices. Any of these specifications could probably be improved by one or two orders of magnitude but with an increase in cost.

The aging history of two types of crystals over a 5000-hour period is shown in Figure 4. The upper curves show the aging data for a sample of 4.7755 MHZ fundamental mode crystals. The lower curves show the aging data for a sample of 108.933 MHZ fifth overtone crystals.

In the design of packet radio systems, the stability of both the clock and the RF carrier are important considerations. Note #40 concerns the clock synchronization.

The stability required of the RF carrier can also be a very important consideration in the design of packet radio systems because frequency uncertainty increases the time required to acquire the signal and/or affects the efficiency of the detection process. The RF stability requirements of the various detection techniques can be a significant factor affecting the choice of modulation technique. This subject is discussed in more detail in Note #33, particularly with regard to stability required for efficient detection using surface acoustic wave correlators.

When microwave sources are to be crystal-controlled, it is convenient to operate the crystal reference oscillator at as high a frequency as possible. Fifth overtone crystal oscillators operating at a frequency near 100 MHZ are typical. A typical source (See Radio Note #15) will employ a crystal oscillator at a suitable frequency in the region of 100 MHZ which produces a spectrum of harmonics. A cavity oscillator in the frequency range of 1 to 2 GHZ is then locked to the appropriate crystal oscillator harmonic using conventional phase lock loop techniques. Further multiplication using varactor multipliers then may be employed to achieve the desired output frequency.

Such microwave sources are not limited to use of high frequency overtone crystals, but their use does considerably simplify the frequency reference since it minimizes the amount of frequency multiplication required and reduces the possibility of false lock on an undesired harmonic. Oscillators operating near 100 MHZ may have 1 to 2 orders of magnitude poorer stability than the best crystals operating at a frequency near 5 MHZ.

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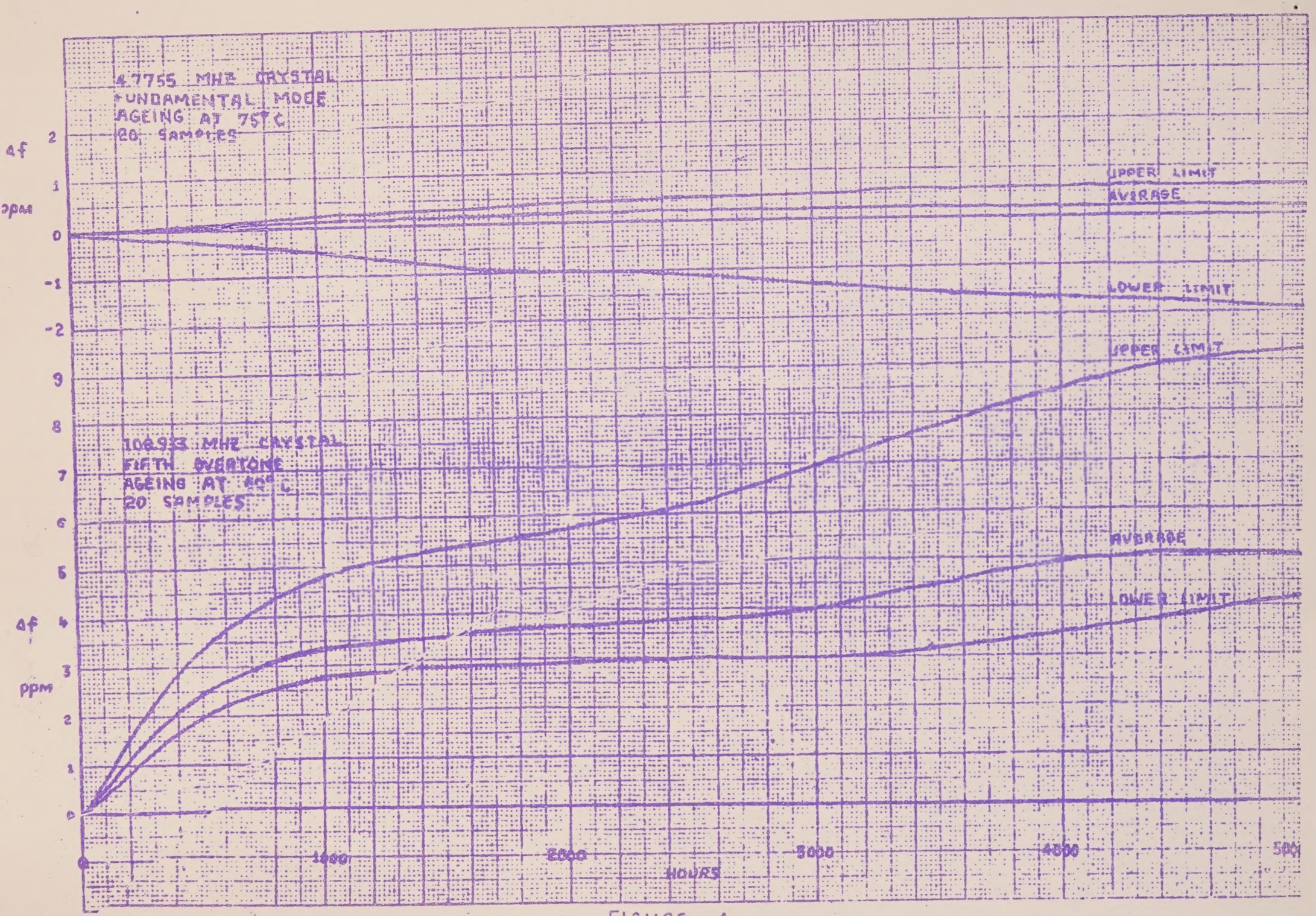
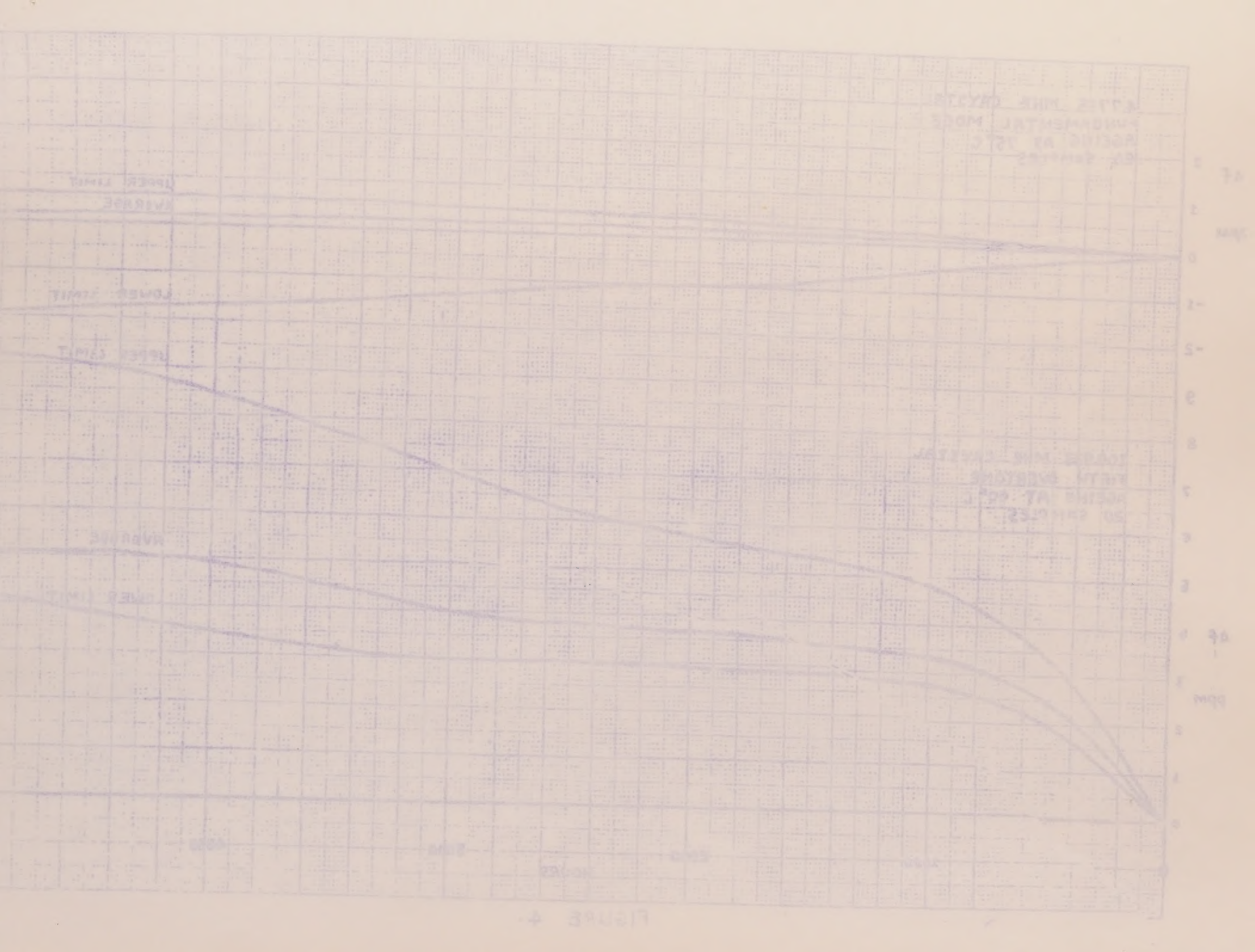


FIGURE 4.



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3. E. A. Gerber and R. A. Sykes, "State of the Art - Quartz Crystal Units and Oscillators," Proceedings of the IEEE, Vol. 54, No.2, pp 103-115, February, 1966